Science & Technology Facilities Council
Rutherford Appleton Laboratory

Microelectronics Support Centre Short Course:

Introduction to FPGA Design Using Xilinx Vivado

Duration: 2 days

Dates: see website

Location: Rutherford Appleton Laboratory

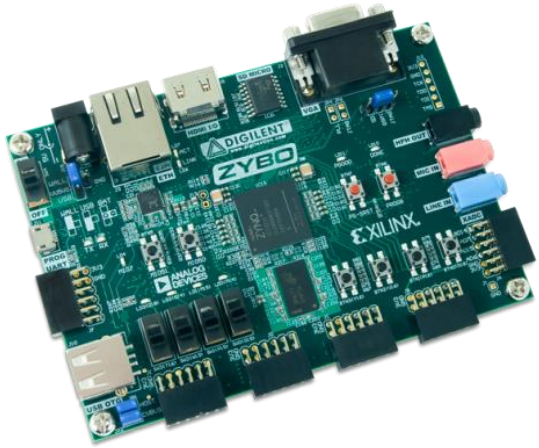
Overview:

This training course provides a comprehensive introduction to the FPGA design flow, from VHDL description through to device programming and hardware debug. The Xilinx Vivado tools are used for all steps in the flow, including synthesis and simulation.

The course includes practical hands-on exercises using a Digilent ZYBO development board to implement, test and debug the design examples. Delegates are free to take this development board away with them at the end of the course.

Topics covered on this course include:

- Xilinx series 7 architecture
- FPGA Design flow
- Synthesis
- Timing analysis
- Constraints
- Clock routing and multiple clock designs
- Xilinx IP generation
- Implementation and on chip debug



Target Audience:

The course is aimed primarily at circuit designers who are FPGA novices, but is also suitable for designers migrating from the Xilinx ISE design flow.

Course Objectives:

Introduction to the complete Vivado design flow, as required to take an HDL design description through to a fully working device.

Course Prerequisites:

The examples in this course are written using VHDL. Familiarity with VHDL may improve your experience but is not required. Other instances of this course are offered with Verilog examples, please see the calendar for dates.

Course examples are run on Linux workstations, but no specialist knowledge of Linux is required.

Full Course Outline

1. Lecture: Xilinx 7 series devices and design flow.
   Lab exercise: Synthesis, implementation, bitstream generation and device programming.

2. Lecture: Vivado design flow.
   Lab exercise: A more detailed design flow including simulation.

3. Lecture: XDC and Timing Constraints.
   Lab exercise: Using XDC and what to do when constraints fail.

4. Lecture: IP Integrator
   Lab exercise: Using the Xilinx IP library and wrapping your own IP.

5. Lecture: Time for Clocks
   Lab exercise: Using Xilinx CMT's and multiple clock regions.

6. Lecture: Vivado project management
   Lab exercise: tcl automation and incremental implementation

7. Lecture: Hardware debug
   Lab exercise: Using Vivado ILA to probe signals in working designs.

8. Lecture: What to do next: an overview of the rest of the Xilinx design space.