



*Microelectronics Support Centre Short Course:*

# **An Introduction to Front End Analogue IC Design Flows in Cadence IC 6.1**

Duration: 3 days

Dates: see website

Location: Rutherford Appleton Laboratory

## **Overview:**

A completely new version of the Custom IC Design Framework (IC 6.1) is available from Cadence, which will replace the previous IC 5.1.41 version. IC 6.1 has a different graphical user interface, based on QT, and a different design database format (OpenAccess) from IC 5.1.41. This course introduces the IC 6.1 environment and shows how to run a variety of different front-end analogue IC design tasks. The course will be presented by staff from the Microelectronics Support Centre at STFC Rutherford Appleton Laboratory and will consist of a mixture of lectures and hands-on labs.

The following topics will be covered in this front-end course:

- Introduction to the IC 6.1 framework and the design database
- Schematic capture and schematic symbol generation
- Running basic simulations and presenting and evaluating the results
- Parametric analysis
- Corners analysis
- Monte Carlo simulation and parametric yield estimation
- Circuit optimisation
- Parametric yield optimisation
- Configurations and hierarchical design.

A companion course introduces the corresponding physical implementation (back-end) flows for analogue ICs.

## **Target Audience:**

This course is aimed at lecturers, researchers and postgraduate students working in analogue IC design who wish to gain an insight into tool methodologies at the front end of the full custom analogue design flow.

## **Course Objectives:**

The aim of this course is to provide attendees with the skills necessary to design and simulate their analogue designs in modern CMOS processes, enabling users to directly apply the knowledge acquired to their own designs after the course.

## **Course Prerequisites:**

The course will be suitable for those with a basic understanding of front-end analogue IC design tasks or those who are already familiar with running such steps in a different EDA environment (including IC 5.1.41). Previous experience of using UNIX/Linux systems will be helpful but not essential.



## Full Course Outline

### Day 1:

- Lecture 1: Introduction to the IC6 Design Framework
  - Lab Exercise: Familiarization with the IC6 DFII Environment
  - Lab Exercise: Creating Libraries
- Lecture 2: Schematic Capture
  - Lab Exercise: Schematic Design Entry
- Lecture 3: Automatic Symbol Generation
  - Lab Exercise: Symbol Creation
  - Lab Exercise: Creating component parameters and building testbenches
  - Lab Exercise: Editing at different levels of hierarchy using the assistants
- Lecture 4: Basic Analogue Simulation
  - Lab Exercise: Simulation of an amplifier design
  - Lab Exercise: Viewing simulation results
  - Lab Exercise: Saving simulation Defaults
  - Lab Exercise: Annotating simulation results to the schematic window

### Day 2:

- Lecture 1: Exploring Simulation Results with the Calculator and Data View Assistant
  - Lab Exercise: The Waveform Calculator
  - Lab Exercise: Managing Simulation Results
  - Lab Exercise: Using the Spectre Sweep Feature
- Lecture 2: The Results Browser and Specifications
  - Lab Exercise: Managing Simulation Data with the Results Browser
  - Lab Exercise: Running Multiple Tests and Using Specifications
- Lecture 3: Advanced Analysis
  - Lab Exercise: Running Parametric Analysis
  - Lab Exercise: Exploring the Model Library Setup
  - Lab Exercise: Running Corner Analysis
- Lecture 4: Advanced Analysis: Monte Carlo
  - Lab Exercise: Running Monte Carlo Analysis

### Day 3:

- Lecture 1: Advanced Analysis: Circuit Optimisation
  - Lab Exercise: Running Local Optimisation
- Lecture 2: Advanced Analysis: Improving Yield
  - Lab Exercise: Parametric Yield Optimisation
- Lecture 3: The Hierarchy Editor
  - Lab Exercise: The Hierarchy Editor
  - Lab Exercise: Creating behavioural models
  - Lab Exercise: Managing configurations and simulating Verilog-A cellviews

### Notes:

The Constraint Manager and parasitic estimation are outside of the scope of this short course.